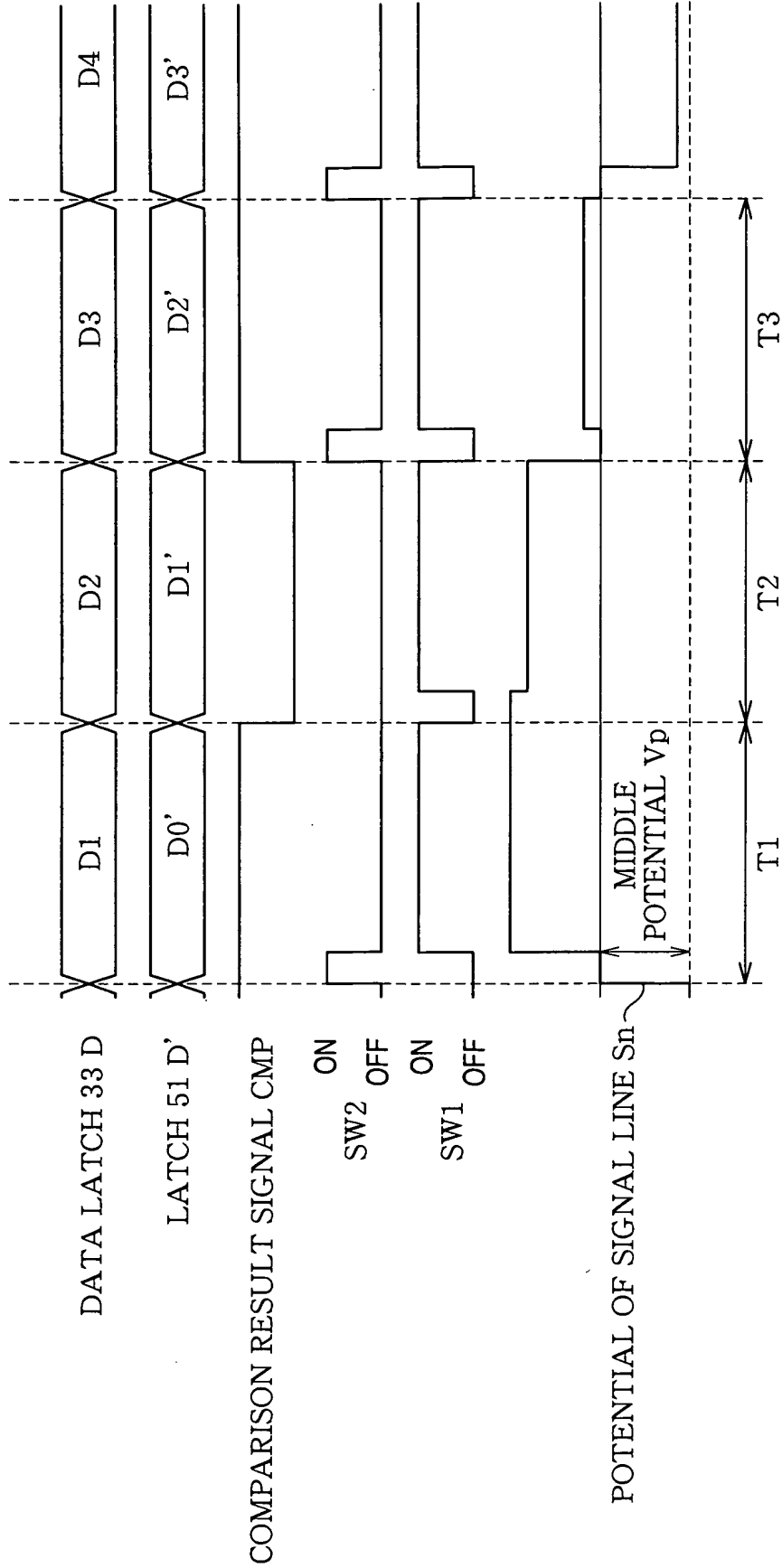


FIG. 1

FIG. 1 is a block diagram of a control circuit. The circuit includes a DATA LATCH (33) which receives input D and LPO. The output of the DATA LATCH (33) is connected to a LATCH (11) and a DECODER (34). The LATCH (11) is connected to a COMPARATOR (12). The DECODER (34) is connected to an ANALOG SWITCH (35). The ANALOG SWITCH (35) is connected to an OUTPUT CIRCUIT (36). The COMPARATOR (12) is connected to a SWITCH CONTROLLER (13). The SWITCH CONTROLLER (13) is connected to two switches, SW1 and SW2. The OUTPUT CIRCUIT (36) is connected to SW1. SW1 and SW2 are connected to a common output terminal Sn. SW2 is also connected to a terminal Vpo.

FIG. 3



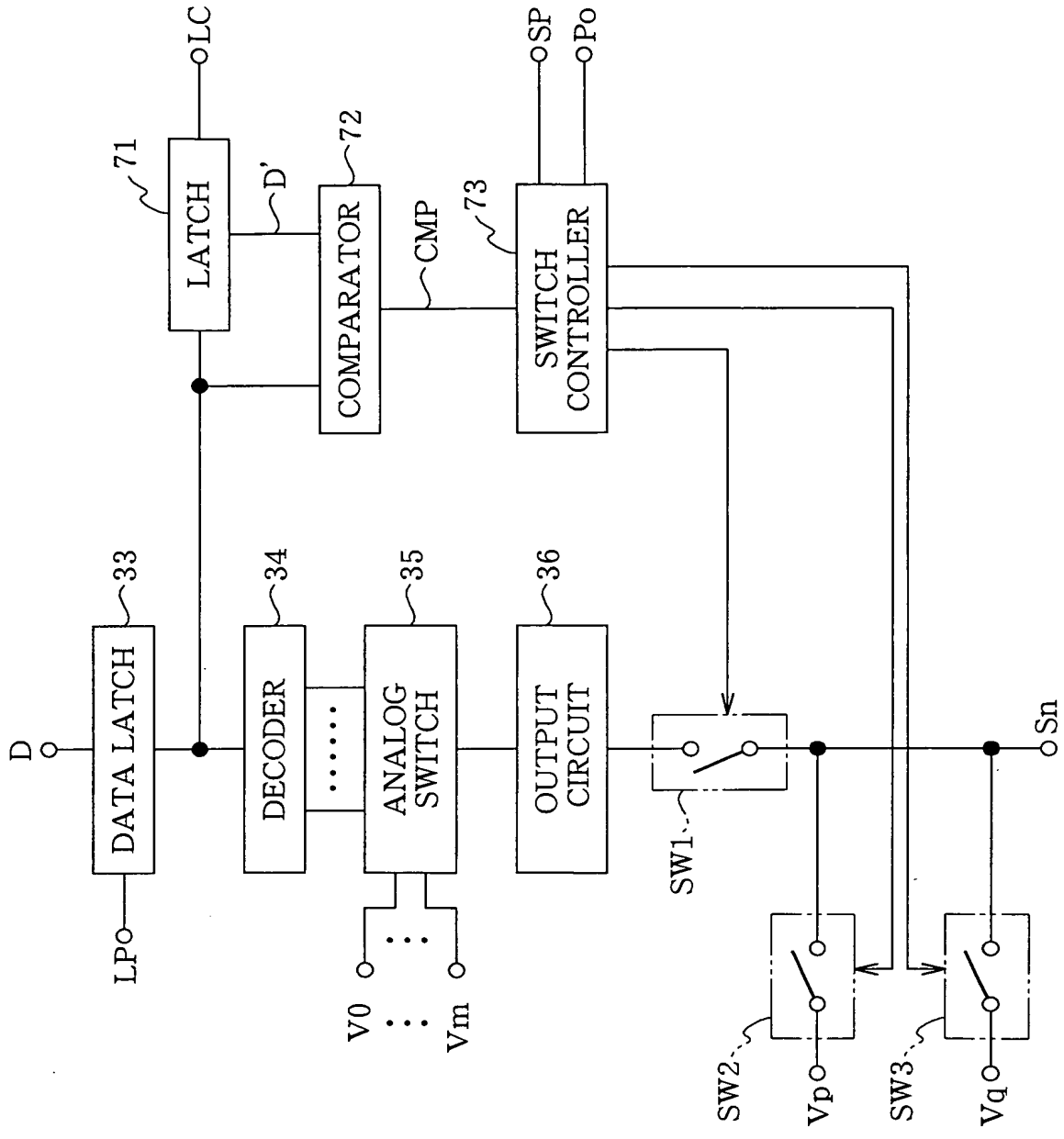
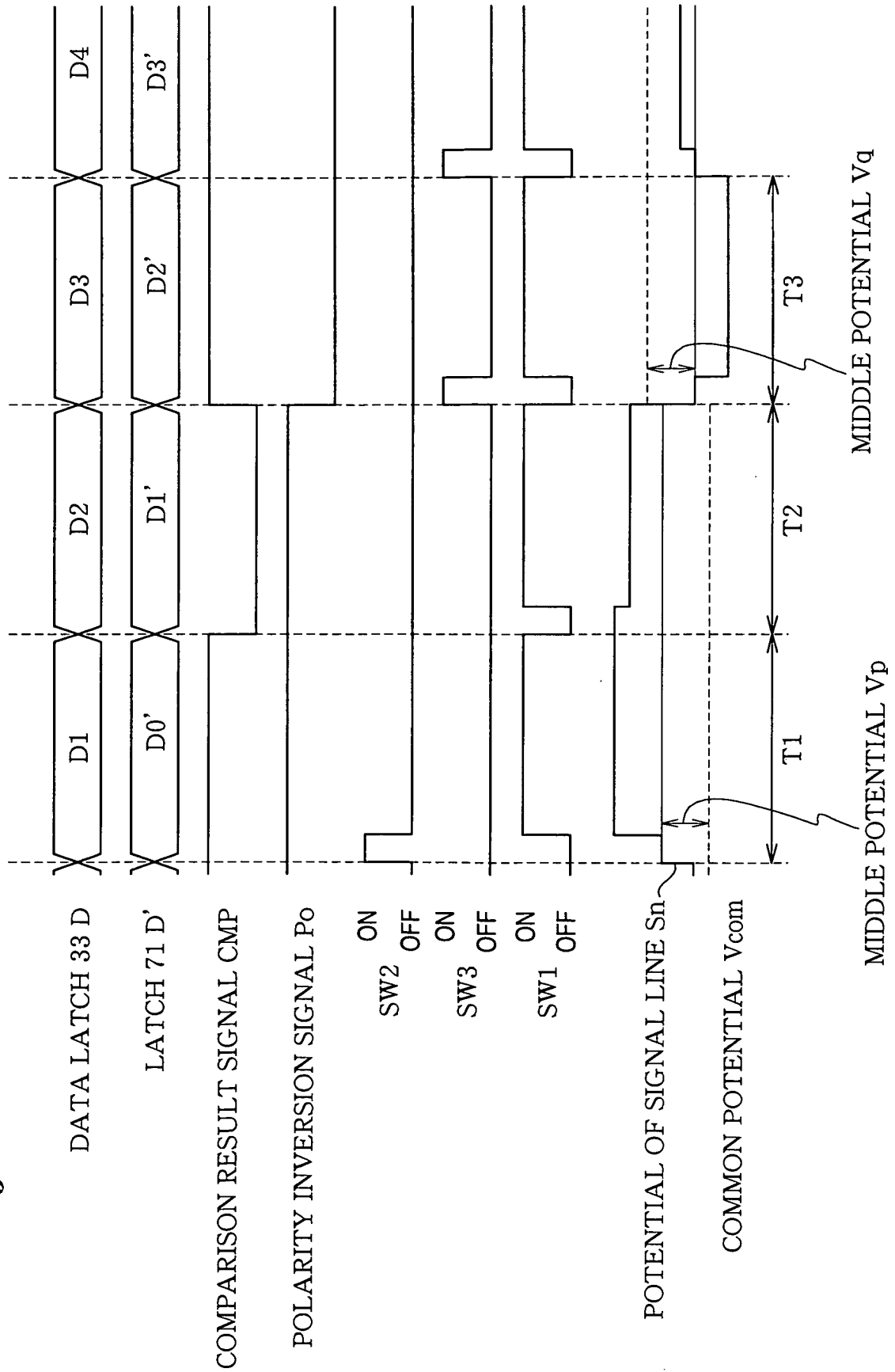


FIG. 4

This drawing is not to scale and is not intended to represent a specific embodiment of the invention. It is merely a schematic diagram of the general principle of the invention.

FIG. 5



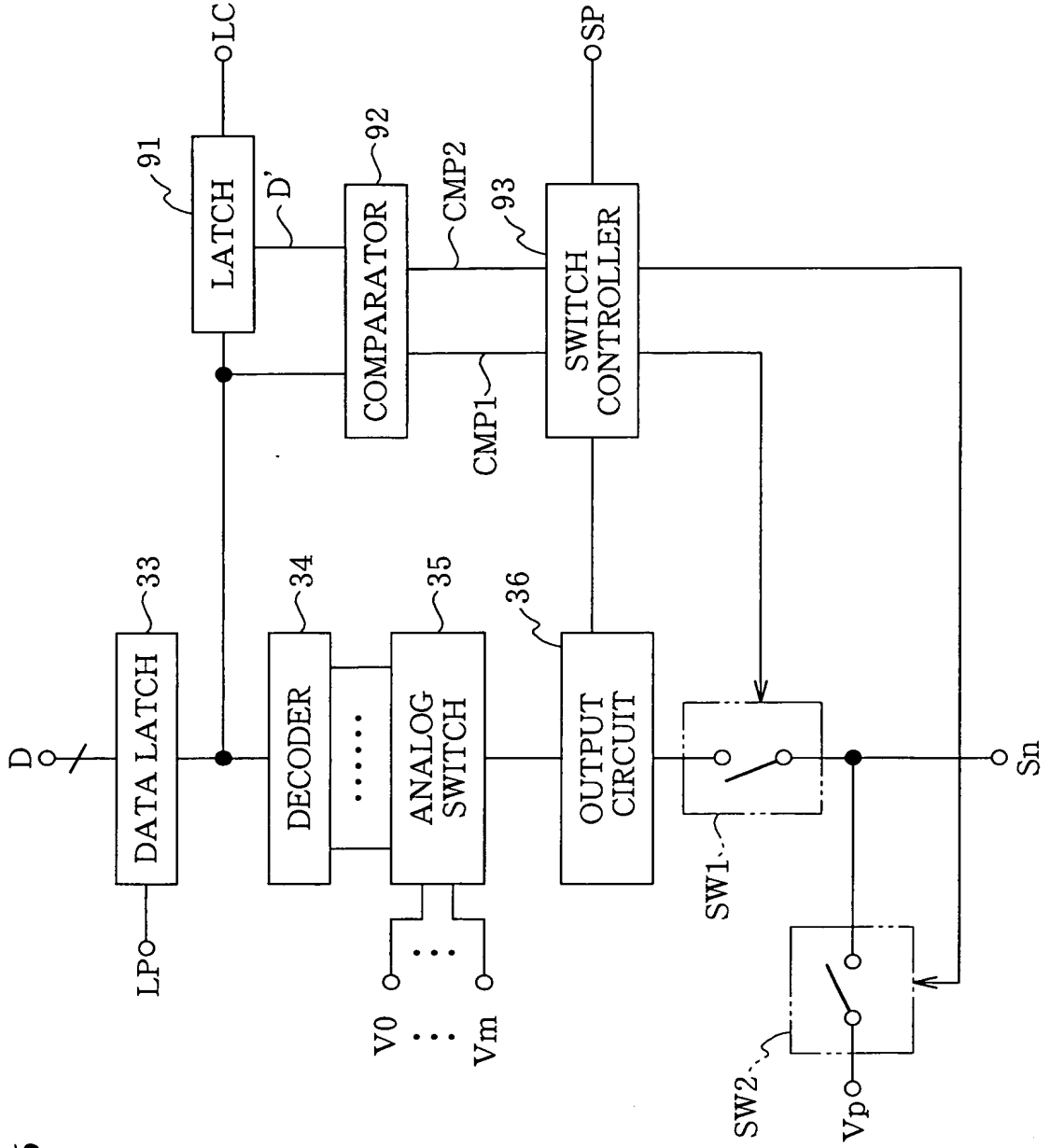


FIG. 6

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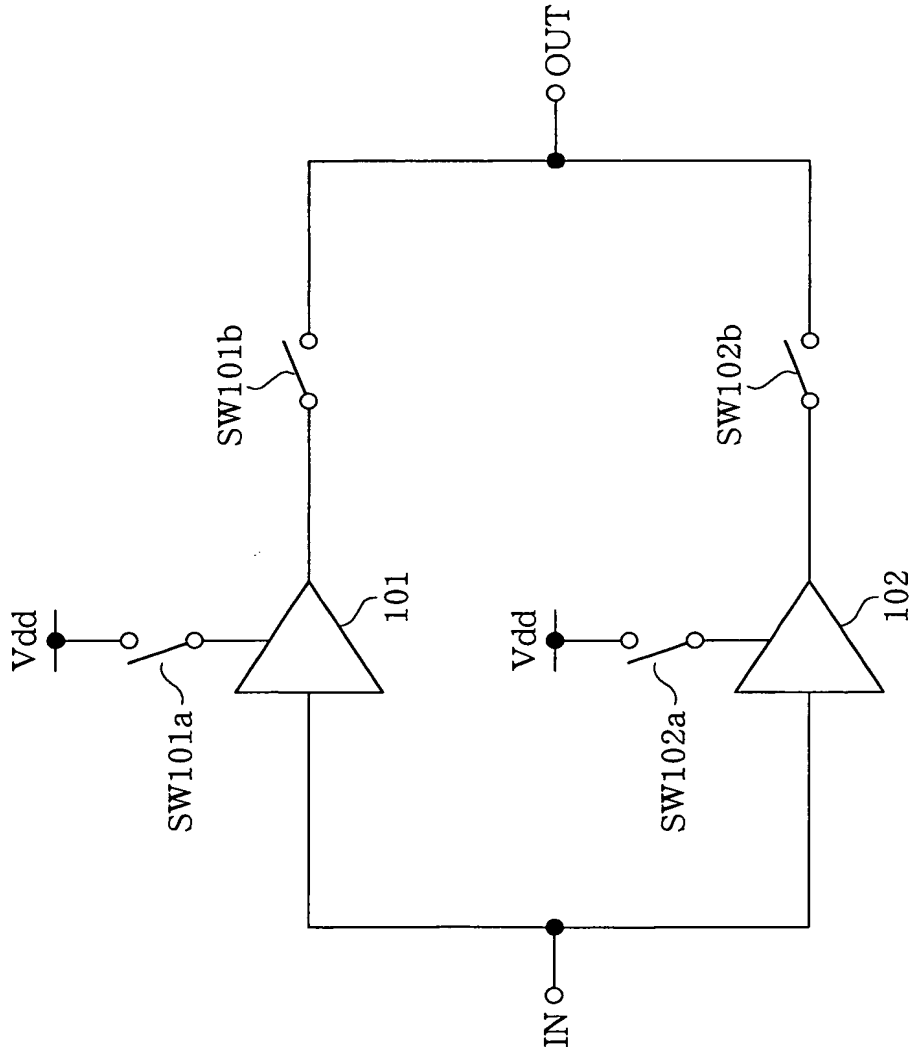


FIG. 7

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FIG. 8

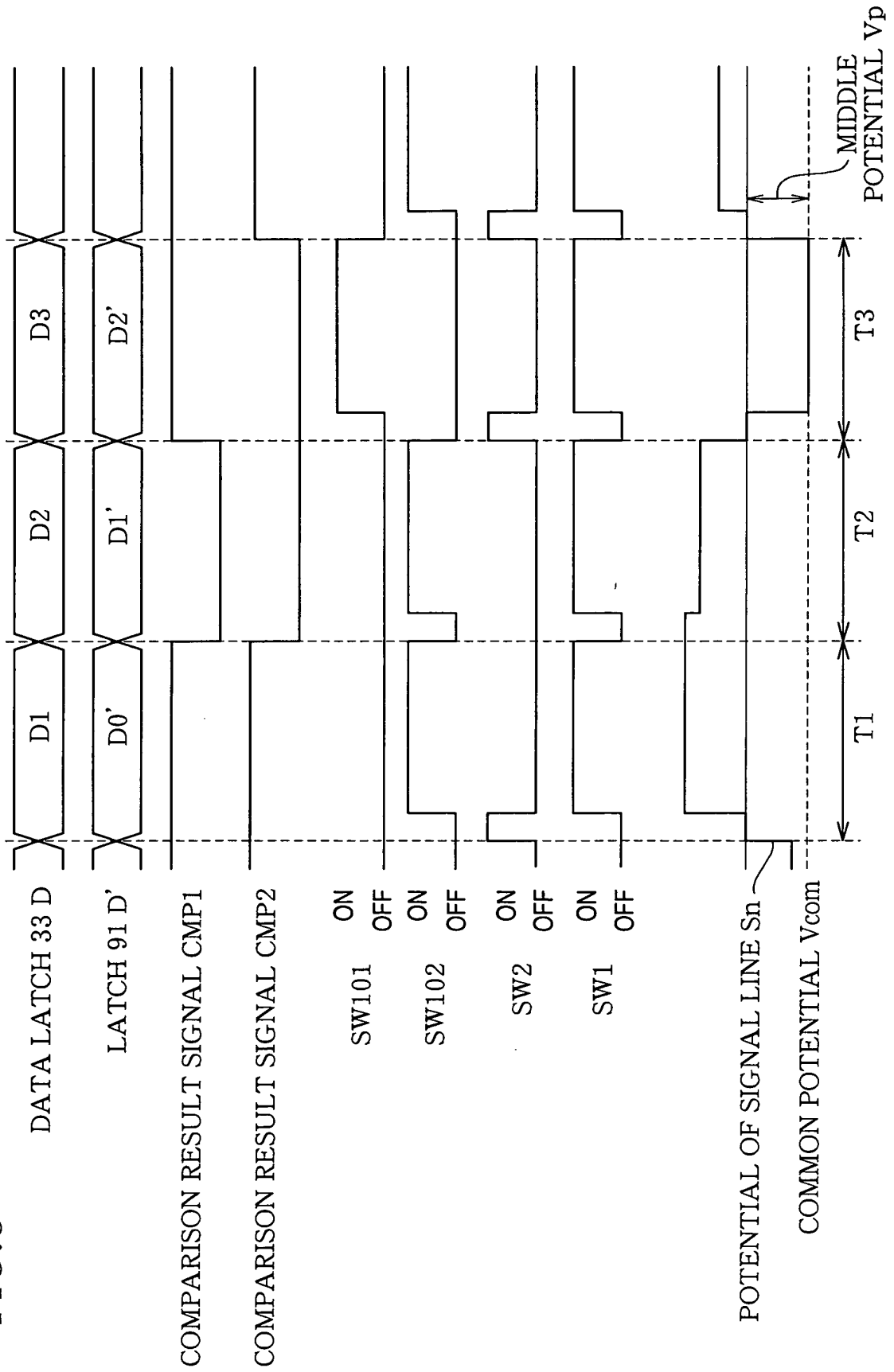


FIG. 9

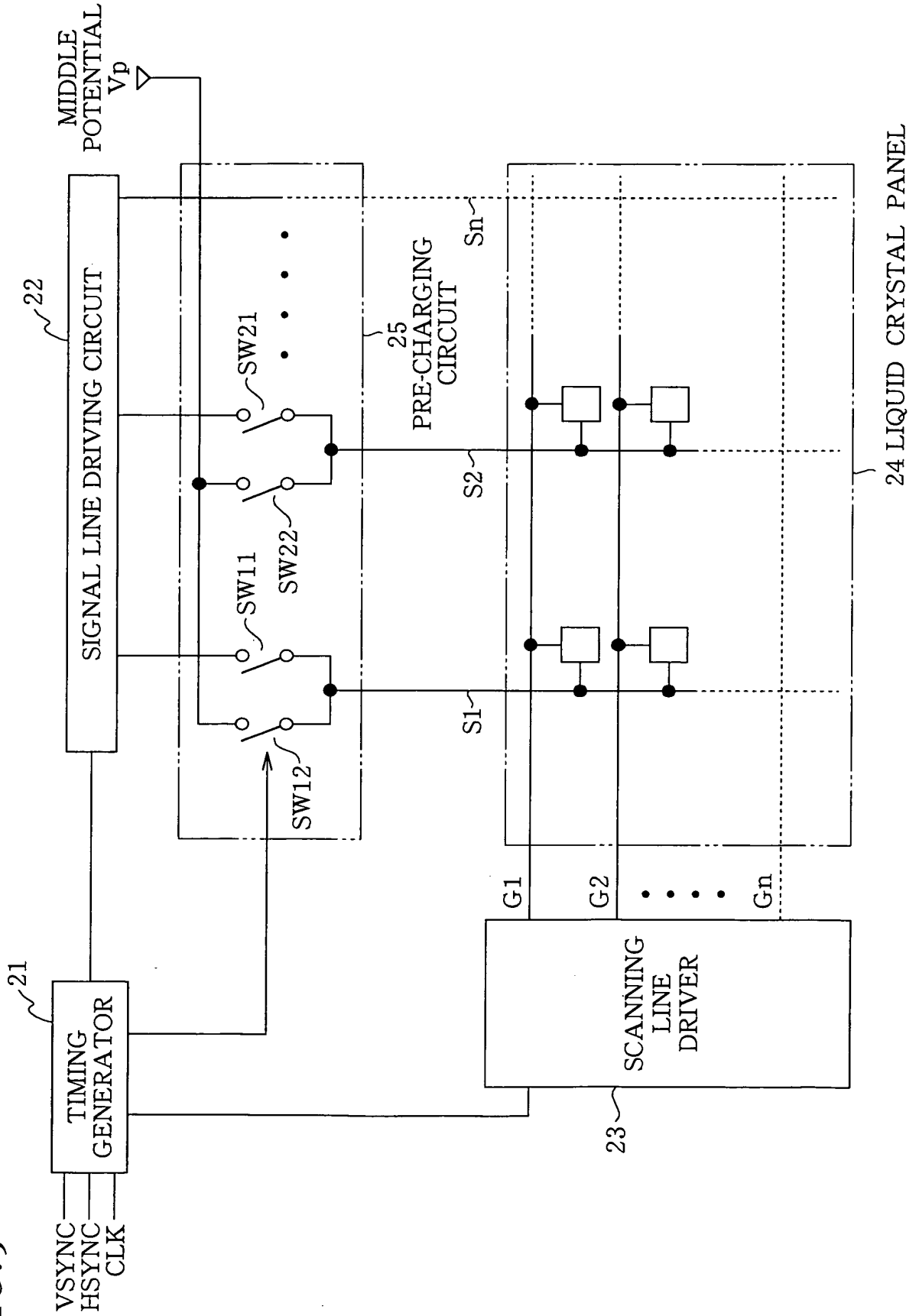
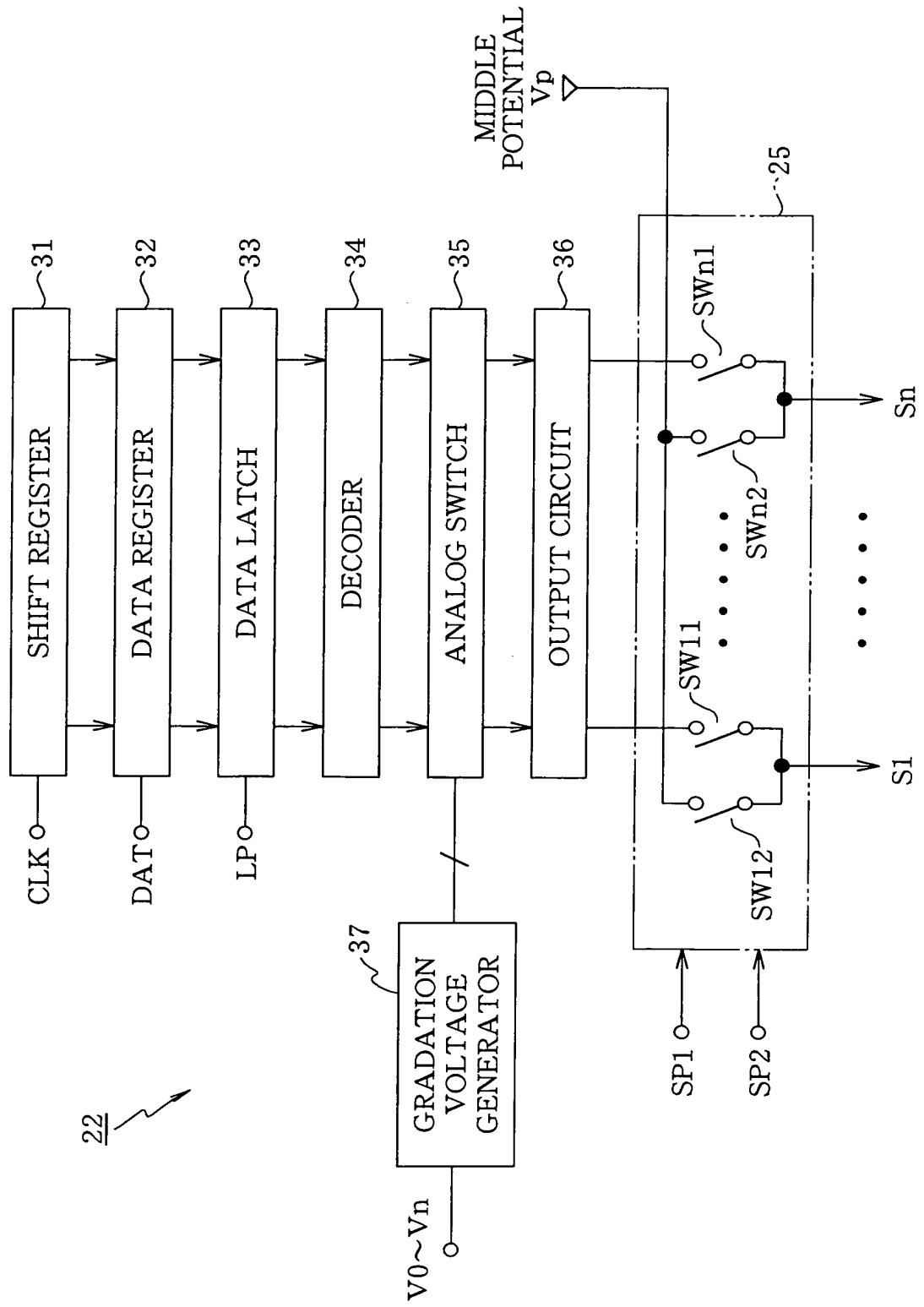


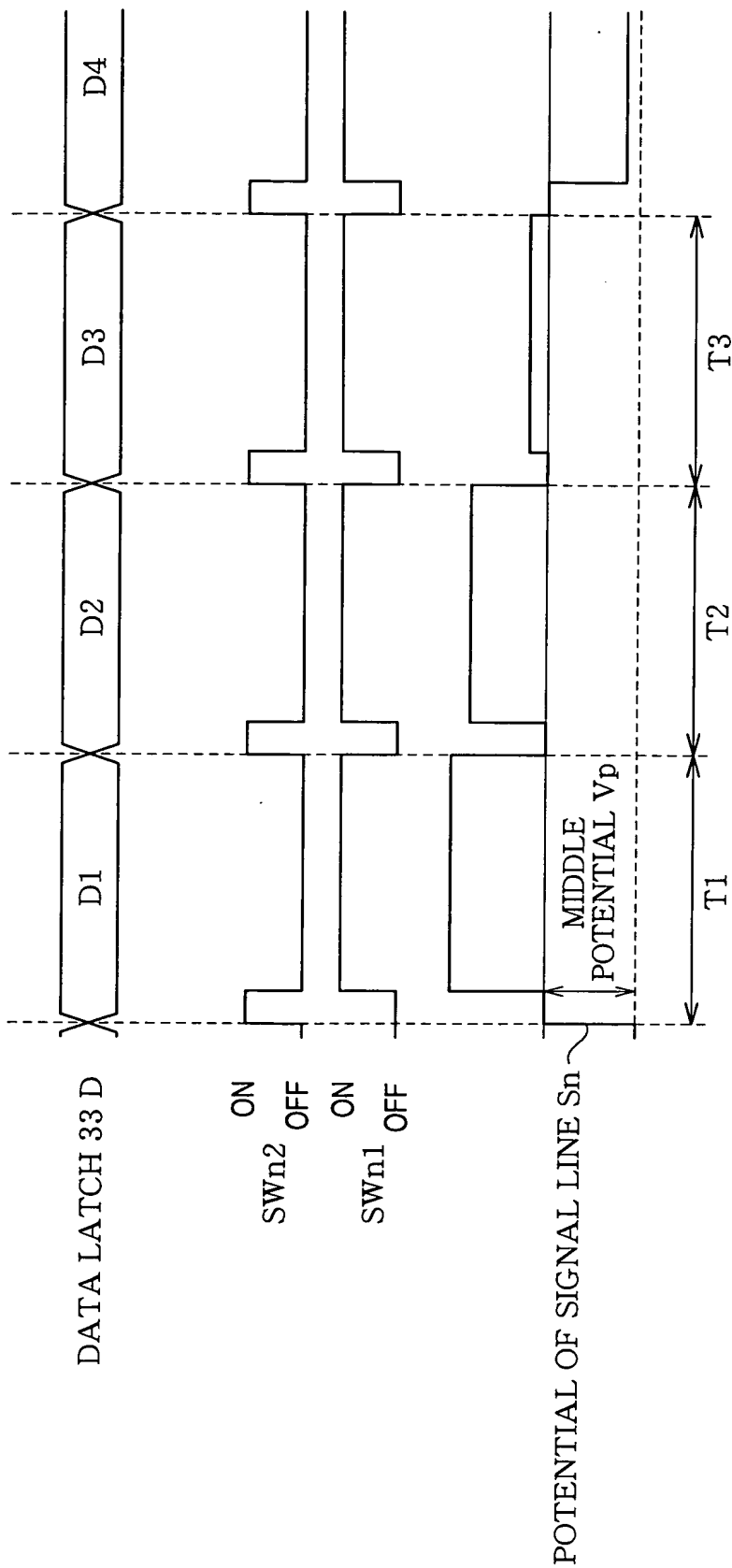
FIG. 10



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FIG. 11



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